Pending Claims

1. (previously presented) An interface device for enabling communications between a host and a subsystem, comprising:

(a) a register set comprising a plurality of registers configurable to control host-subsystem communications according to a UART standard;

(b) a host interface configurable to establish data communication with the host;

(c) a serial interface configurable to establish a bi-directional serial data communication channel to the subsystem under control of the register set; and

(d) a parallel interface configurable to establish an auxiliary parallel data communication channel to the subsystem operable in conjunction with the serial data communication channel, wherein the parallel interface operates under control of the register set.

2. (cancelled)

3. (original) An interface device according to claim 1, further comprising a supplementary data buffer for writing and/or reading data to and/or from the subsystem via the parallel interface.

4. (original) An interface device according to claim 3, wherein one of the registers is mapped to the data buffer so that accesses to the mapped register will cause accesses to the data buffer.

5. (original) An interface device according to claim 3, wherein the data buffer is a FIFO buffer.

6. (previously presented) An interface device according to claim 1, further comprising supplementary data buffers for writing and reading data to and from the subsystem via the parallel interface.

7. (original) An interface device according to claim 6, wherein one of the registers is mapped to at least one of the supplementary data buffers so that accesses to the mapped register will cause accesses to the at least one of the supplementary data buffers.

8. (original) An interface device according to claim 6, wherein the data buffers are FIFO buffers.

9. (previously presented) An interface device according to claim 6, further comprising first control and status lines connected between each data buffer and the register set to communicate control and status signals to and from each data buffer.

10. (previously presented) An interface device according to claim 9, further comprising second control and status lines connected between each data buffer and the parallel interface to communicate control and status signals to and from each data buffer.

11. (original) An interface device according to claim 1, wherein the UART standard is the 16550 standard.

12. (original) A card comprising an interface device according to claim 1 integrated with a subsystem.

13. (original) A card according to claim 12, wherein the subsystem includes a wireless interface for communicating with a third party data transceiver.

14. (original) A system comprising a host, a subsystem and an interface device according to claim 1 connected between the host and subsystem.

15. (original) A system according to claim 14, wherein the serial data communication channel and the auxiliary parallel data communication channel include wireless portions.

16. (original) A system according to claim 14, wherein the serial data communication channel and the auxiliary parallel data communication channel are made exclusively of fixed links.

17. (previously presented) A method of communicating data between a host and a subsystem, comprising:

(a) establishing a bi-directional serial data communication link with the subsystem under control of a register set conforming to a UART standard;

(b) establishing an auxiliary parallel data communication link with the subsystem also under control of the register set; and

(c) transferring data over the auxiliary parallel data communication link to bypass the serial data communication link.

18. (cancelled)